REMARKS

The present response amends the specification, drawings, and claims 1-6, 10, 11, and 19. In addition, claims 21-22 are added. Claims 1-22 are pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Objection to the Drawings

An objection was lodged against the drawings for failing to indicate Figs. 1-4 as "Prior Art." In response thereto, Figs. 1-4 have been amended as suggested by the Examiner.

In addition, an objection was lodged against the drawings as failing to comply with 37 C.F.R. § 1.84(p)(5). Specifically, the Examiner states that elements 26, 28, 30, and 32 of Fig. 1; elements 22a, 22b, 22c, and 20d of Fig. 3; and element 72 of Fig. 7 are not described in the specification.

In response thereto, Applicants direct the Examiner to the specification, page 5, lines 14-20, for a description of Fig. 1 including elements 26 (single word instruction), 28 (double-word instruction), 30 (op code for single word instruction), and 32 (op code for double-word instruction). In addition, the specification has been amended to more fully describe Fig. 3 and to correct a typographical error on page 16, line 6, which is element 72 of Fig. 7.

Applicants appreciate the Examiner's thorough review of the specification and drawings. In view of the remarks and amendments, Applicants respectfully request removal of this objection.

Section 103 Rejection

Claims 1-6, 8-15, and 17-20 were rejection under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,835,746 to Girardeau, Jr. et al. (hereinafter "Girardeau") in view of an article entitled "Binary Decision Tree Test Function" by S. Aborhey (hereinafter "Aborhey"). In addition, claims 7 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Girardeau, Aborhey, and Applicant's admitted prior art (hereinafter "Prior Art"). To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second,

there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicants contend that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

The cited art does not teach or suggest a binary decision tree having nodes arranged from a top-most node to bottom-most node representing successively preceding memory address locations relative to an address location requested by a microprocessor (claim 1); nor does the cited art teach or suggest a top node of a tree corresponding to a first preceding address location immediately preceding an address location requested by a microprocessor (claims 10 and 19). Each of the present independent claims 1, 10, and 19 define a binary decision tree. Within the binary decision tree is a set of nodes. The nodes are arranged throughout the tree from a top-most node to a bottom-most node. Illustration of a binary decision tree is set forth in Fig. 7 and the relevant portions of the present specification describing Fig. 7. As shown in Fig. 7, the top-most node 76 is at the top level of the tree and represents a memory address immediately preceding a memory address requested by a microprocessor. Thus, if a microprocessor requests address 4004h, then node 76 will correspond to address 4003h and is designated as having a corresponding instruction i-1. *See, e.g.,* the present specification at page 15, line 25 - page 16, line 25.

Extending downward from the top-most node 76 are nodes 82 and 84 representing the next preceding memory address, immediately preceding the address for instruction i-1, thereby indicating nodes 82 and 84 correspond to instruction i-2. Thus, since the memory address requested by the microprocessor corresponds to instruction i, the sequentially preceding memory addresses begin with i-2, then i-3, and so forth to the bottom-most node. The top node, however, corresponds to the first preceding address location that immediately precedes the address location requested by the microprocessor.

Contrary to the present independent claims, Girardeau makes no mention of a binary decision tree. Specifically, Girardeau makes no mention of even the possibility of looking at preceding memory address locations -- i.e., memory address locations that precede the address location requested by a microprocessor.

In fact, all examples given in Girardeau would lead one skilled in the art to focus solely on decoding subsequent pointer count numbers or address locations, not successively preceding memory address location. A skilled artisan reading Girardeau would, therefore, not be motivated in any fashion to modify Girardeau with a binary decision tree, much less a binary decision tree that looks at successively preceding memory addresses corresponding to nodes of that tree.

The shortcomings of Girardeau are compounded by Aborhey. Not only does Aborhey lack any teachings of nodes dedicated to successively preceding memory address locations and corresponding instruction, but makes no mention of its decision tree being possibly used to ascertain single-word or double-word instructions. Since Aborhey makes no mention of addresses and corresponding instruction being associated with nodes, Aborhey certainly could not make any suggestion of using a binary tree for the presently claimed purpose. Thus, the combination of Girardeau and Aborhey cannot be successfully made since there are no teachings or suggestions in either reference that would motivate a skilled artisan to make the hypothetical combination suggested by the Examiner.

The cited art does not teach or suggest using a decision tree to determine whether an instruction corresponding to an address location immediately preceding the address location requested by the microprocessor is a single-word or a double-word instructions, depending on whether tests performed on at least two nodes lower than the top-most node determines that the instructions corresponding to at least two successively preceding memory address locations contain the marker bit pattern (claim 1, 10, and 19). Not only do the independent claims recite a binary decision tree with nodes and corresponding successively preceding memory address locations, but also describe the use of the preceding memory address locations. Specifically, each of the independent claims define logic used to determine whether an instruction of an address immediately preceding the requested address is a single-word or a double-word instruction. That test is performed in the nodes of the binary decision tree and, specifically, at nodes lower than the top-most node. When applying the logic function, the tests can determine whether the address location immediately preceding the requested address location is a single-word or a double-word instruction depending on whether at least two successively preceding memory address locations contain a marker bit pattern.

Fig. 7 of the present specification illustrates a binary decision tree and the outcome of all possible tests performed at each node of that tree. For example, it cannot be ascertained whether the immediately preceding address of instruction I_1 is a single-word or a double-word instruction until tests are performed in

the second immediately preceding address location for instruction i-3. For example, at node 90 when the test is run for instruction i-3, it is determined that instruction i-1 is a single-word instruction. The right-hand side of Fig. 7 at the node beneath node 84, it can be determined that since the test at instruction i-1 yields "1" and the test at instruction i-2 yields "1," then at instruction i-3, instructions i-1 and i-2 constitute a double-word instruction. Details of how a binary decision tree is used to ascertain the boundary of single-word and double-word instructions are set forth in the originally filed specification, beginning on page 15, line 25. Figs. 8 and 9 of the present specification illustrate determination of the boundaries of single-word instructions and the boundaries of single-word instructions and double-word instructions, respectively. Description of these examples are set forth in the present specification, beginning on page 18, line 18 through page 20, line 21.

In all instances described in the present specification and illustrated in the drawings, however, a system and method are shown for pre-decoding not in the forward pointer address locations, but in the backward pointer address locations. Conventional pre-decoders, such as Girardeau, specifically address forward pre-decoding by looking at an operand of an instruction to determine whether, for that instruction, a single-word or a double-word is involved. Thereafter, the pointer will increment to the next address thereby retrieving that address into one or both multiplexers of Girardeau, depending on whether the instruction contains code representative of a single-word or a double-word. This process is continued for each count increment of memory addresses fetched from the memory to the multiplexers. Converse to the forward pre-decoding of Girardeau, the present claims deal with looking at instructions prior to the pointer count value so that if a loop or branch is encountered (as shown in Fig. 3), the entire block of address locations are pre-decoded and ready for placement into the cache absent incurring a cache miss as in conventional systems which can only forward pre-decode. Details of the differences between backward pre-decoding and forward pre-decoding is set forth in reference to the background section of the present specification compared to the summary section of the present specification. Moreover, the novel mechanism by which a binary decision tree is used is described fully with reference to numerous examples, beginning with the examples of the trees shown in Figs. 7-9.

For at least the foregoing reasons, Applicants assert that independent claims 1, 10, and 19, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed September 16, 2004. In view of the remarks traversing rejections, Applicants assert that pending claims 1-22 are in condition for allowance. If the Examiner has any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to deposit account number 12-2252/ 01-577.

Respectfully submitted,

Kevin L. Daffer
Reg. No. 34,146
Attorney for Applicant(s)

Daffer McDaniel, LLP
P.O. Box 684908
Austin, TX 78768-4908
(512) 476-1400
Date: December 14, 2004

Amendments to the Drawings

Attached are replacement sheets for Figs. 1-11. Amendments have been made only to Figs. 1-4 to indicate them as "Prior Art." No further changes have been made to the drawings. Approval of the amended drawings is respectfully requested.

Attachment: Replacement sheets, Figs. 1-11.